



# 218  
# 15

PATENT APPLICATION

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of      Ryan N. RAKVIC et al.  
Group Art Unit:                2188  
Application No.:              09/891,523  
Examiner:                     Midys INOA  
Filed:                        June 27, 2001  
Docket No.:                   02207/1123601  
For:                          Parallel Cachelets

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Technology Center 2100

INFORMATION DISCLOSURE STATEMENT

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P.O. Box 1450  
Alexandria, VA 22313-1450

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2. This Information Disclosure Statement is being filed more than three months after the U.S. filing date AND after the mailing date of the first Office Action on the merits, but before the mailing date of a final action, Notice of Allowance, or any action that otherwise closes prosecution.

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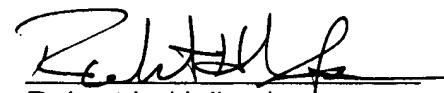
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■ c. Please debit Deposit Account No. 11-0600 in the amount of \$180.00 in payment of the fee under 37 CFR §1.17(p) to ensure consideration of the disclosed information. Two duplicate copies of this paper are attached. 37 CFR §1.97(c)(2).

Respectfully submitted,

KENYON & KENYON

Date: 3/31/04



Robert L. Hails, Jr.  
Registration No. 39,702

Kenyon & Kenyon & Kenyon  
1500 K Street, N.W.  
Washington, D.C. 20005  
Telephone: (202) 220-4200  
Facsimile: (202) 220-4201

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<b>INFORMATION DISCLOSURE STATEMENT BY APPLICANT</b> <i>(Use as many sheets as necessary)</i>		Application Number	09/891,523
		Filing Date	June 27, 2001
		First Named Inventor	Ryan N. RAKVIC et al.
		Art Unit	2188
		Examiner Name	Midys INOA
		Attorney Docket Number	02207/1123601
Sheet	1	of	2

## **U.S. PATENT DOCUMENTS**

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## FOREIGN PATENT DOCUMENTS

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This collection of information is required by 37 CFR 1.97 and 1.98. The information is required to obtain or retain a benefit by the public which is to file (and by the USPTO to process) an application. Confidentiality is governed by 35 U.S.C. 122 and 37 CFR 1.14. This collection is estimated to take 2 hours to complete, including gathering, preparing, and submitting the completed application form to the USPTO. Time will vary depending upon the individual case. Any comments on the amount of time you require to complete this form and/or suggestions for reducing this burden, should be sent to the Chief Information Officer, U.S. Patent and Trademark Office, U.S. Department of Commerce, P.O. Box 1450, Alexandria, VA 22313-1450. DO NOT SEND FEES OR COMPLETED FORMS TO THIS ADDRESS. SEND TO: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450, DC01487788 v1.



PTO/SB/08b(08-03)

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2

of

2

## Complete if Known

Application Number

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First Named Inventor

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Art Unit

2188

Examiner Name

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Technology Center 2100

Attorney Docket Number

02207/1123601

NON PATENT LITERATURE DOCUMENTS				
Examiner Initials *	Cite No. <sup>1</sup>	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.		T <sup>2</sup>
	9	BLACK et al, "The Block-Based Trace Cache", Proceedings of The 26th Int'l. Symposium on Computer Architecture, pp. 196-207, May 2-4, 1999, Atlanta, Georgia		
	10	CONTE et al, "Optimization of Instruction Fetch Mechanisms for High Issue Rates", Proceedings of the 22nd Annual Int'l Symposium on Computer Architecture, pp. 333-344, June 22-24, 1995, Santa Margherita Ligure, Italy		
	11	DUTTA et al, "Control Flow Prediction with Tree-Like Subgraphs for Superscalar Processors", Proceedings of The 28th Int'l. Symposium on Microarchitecture, pp. 258-263, Nov. 29 - Dec. 1, 1995, Ann Arbor, Michigan		
	12	FRIENDLY et al, "Alternative Fetch and Issue Policies for the Trace Cache Fetch Mechanism", Proceedings of The 30 <sup>th</sup> Annual IEEE/ACM Int'l Symposium on Microarchitecture, pp. 24-33, Dec. 1-3, 1997, Research Triangle Park, North Carolina		
	13	INTRATER et al, "Performance Evaluation of a Decoded Instruction Cache for Variable Instruction-Length Computers", Proceedings of the 19 <sup>th</sup> Annual Int'l Symposium on Computer Architecture, pp. 106-113, May 19-21, 1992, Gold Coast, Australia		
	14	JACOBSON et al, "Path-Based Next Trace Prediction", Proceedings of the 30 <sup>th</sup> Annual Int'l Symposium on Microarchitecture, pp. 14-23, December 1-3, 1997, Research Triangle Park, North Carolina		
	15	MCFARLING, SCOTT, "Combining Branch Predictors", June, 1993, WRL Technical Note TN-36, Digital Western Research Laboratory, pp. i-25, Palo Alto, California		
	16	MICHAUD et al, "Exploring Instruction-Fetch Bandwidth Requirement in Wide-Issue Superscalar Processors", Proceedings of the 1999 Int'l Conference on Parallel Architectures and Compilation Techniques, pp. 2-10, October 12-16, 1999, Newport Beach, California		
	17	PATEL et al, "Improving Trace Cache Effectiveness with Branch Promotion and Trace Packing", Proceedings of The 25 <sup>th</sup> Annual Int'l Symposium on Computer Architecture, pp. 262-271, June 27 – July 1, 1998, Barcelona, Spain		
	18	REINMAN et al, "A Scalable Front-End Architecture for Fast Instruction Delivery", Proceedings of the 26 <sup>th</sup> Int'l Symposium on Computer Architecture, pp. 234-245, May 2-4, 1999, Atlanta, Georgia		
	19	ROTBENBERG et al, "Trace Cache: A Low Latency Approach to High Bandwidth Instruction Fetching", Proceedings of the 29 <sup>th</sup> Annual IEEE/ACM Int'l Symposium on Microarchitecture, MICRO-29, pp. 24-34, December 2-4, 1996, Paris, France		
	20	SEZNEC et al, "Multiple-Block Ahead Branch Predictors", Proceedings of the 7 <sup>th</sup> Int'l Conference on Architectural Support for Programming Languages and Operating Systems, pp. 116-127, October 1-4, 1996, Cambridge, USA		
	21	YEH et al, "Increasing the Instruction Fetch Rate via Multiple Branch Prediction and A Branch Address Cache", Proceedings of the 7 <sup>th</sup> Int'l Conference on Supercomputing, pp. 67-76, July 1993, Ann Arbor, Michigan		

Examiner Signature	Date Considered
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